Claims

We claim:

1. A method for fabricating a transistor on a semiconductor substrate, comprising the steps of:

forming a first oxide layer on the substrate;

forming a second oxide layer on the substrate; and

forming a gate over the substrate

wherein the first oxide layer and the second oxide layer form a composite oxide layer under the gate, the composite oxide layer being thicker near at least one end of the gate.

2. The method of claim 1 wherein the step of forming the first oxide layer further comprises:

forming an initial oxide layer that uniformly covers an active area of the transistor; and

etching away the initial oxide layer in most of the active area, leaving a portions of the initial oxide layer in a location over which a part the gate is formed.

3. The method of claim 2 wherein the step of etching away an area of the inital oxide layer to create the first oxide layer is performed using a low voltage mask that covers a portion of the active area near where an end of the gate is formed.

4. The method of claim 3 wherein the portions of the active area covered by the low voltage mask extends beyond sides of the gate.

5. The method of claim 1 further comprising forming lightly doped drain regions of the transistor by implanting dopants through the composite oxide layer, wherein the dopants are partially blocked or attenuated during the implant by the thicker composite oxide layer near an end of the gate.

6. The method of claim 1 further comprising forming spacers adjacent the gate.

7. The method of claim 1 further comprising forming source and drain regions of the transistor by implanting dopants through the composite oxide layer, wherein the dopants are partially blocked or attenuated during the implant by the thicker composite oxide layer near an end of the gate.

8. The method of claim 1 wherein the step of forming the first oxide layer comprises;

placing a mask over the substrate, the mask covering most of an active area of the transistor, leaving exposed to an oxidation ambient a portion of the active area in a location over which a part the gate is formed.; and

oxidizing the substrate in the oxidation ambient to form the first oxide layer.

9. The method of claim 1 wherein the step of forming the second oxide layer further comprises;

placing a mask over the substrate, the mask covering most of an active area of the transistor, leaving exposed to an oxidation ambient a portion of the active area in a location over which a part the gate is formed.; and

oxidizing the substrate in the oxidation ambient to form the second oxide layer.

10. A transistor fabricated on a semiconductor substrate, comprising:

a gate over the substrate;

a source region and a drain region in the substrate on opposite sides of the gate; and

a composite gate oxide layer having non-uniform thickness under the gate.

11. The method of claim 10 wherein the composite oxide layer is thicker near at least one end of the gate, causing greater separation of the gate from the substrate near that end.

12. The transistor of claim 11 wherein a length of a thicker portion of the composite gate oxide is longer than the length of the gate so that the thicker portion of the composite gate oxide extends beyond two sides of the gate.

13. The transistor of claim 11 wherein the transistor is adjacent to at least two isolation regions in the substrate and the gate extends from one isolation region to another isolation region.

14. The transistor of claim 13 wherein the composite gate oxide is thicker adjacent to the isolation regions.

15. The transistor of claim 10 wherein the composite gate oxide comprises a first oxide layer and a second oxide layer, the first oxide layer being nearly uniform under the gate and the second oxide layer only covering a portion of the first oxide layer under the gate.

16. The transistor of claim 10 further comprising spacers adjacent the gate.

17. The transistor of claim 10 wherein doping concentrations in the source or drain region are lighter near ends of the gate.

18. The transistor of claim 10 further comprising lightly doped drain regions adjacent the source and drain regions.

19. The transistor of claim 18 wherein doping concentrations in the lightly doped drain regions are lighter near ends of the gate.